

REMARKS

Claims 1 - 17 are pending in the referenced application.

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 101 Rejections

Examiner rejected claims 1-17 under 35 U.S.C. 101 as claiming the same invention as that of claims 1-17 of prior U.S. Patent No. 6,275,240 (hereinafter Riffault).

The foregoing claims have been amended. Applicant respectfully submits that the rejection under 35 U.S.C. 101 as claiming the same invention as that of claims 1-17 of prior U.S. Patent No. 6,275,240 (hereinafter Riffault), is overcome.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call John Ward at (408) 720-8300, x237.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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ATTACHMENT A

A marked-up version of the amended claims is as follows:

1. (Amended) An apparatus [graphics device], comprising:
 - a bus interface unit including a plurality of bus signal buffers to couple the graphics device to a graphics bus; and
 - a load balancing bus signal buffer to further couple the graphics device to the graphics bus, the load balancing bus signal buffer to provide load balancing on the graphics bus when a second graphics device is installed.
2. (Amended) The apparatus [graphics device] of claim 1, wherein the graphics bus is an accelerated graphics port (AGP) bus.
3. (Amended) The apparatus [graphics device] of claim 2, wherein the graphics device is an AGP 2X device.
4. (Amended) The apparatus [graphics device] of claim 3, wherein the upgrade graphics device is an AGP 4X device.
5. (Amended) The apparatus [graphics device] of claim 4, the load balancing bus signal buffer to provide load balancing for a first address/data bus strobe complement signal on the AGP bus.

6. (Amended) The apparatus [graphics device] of claim 4, the load balancing bus signal buffer to provide load balancing for a second address/data bus strobe complement signal on the AGP bus.

7. (Amended) The apparatus [graphics device] of claim 4, the load balancing bus signal buffer to provide load balancing for a sideband strobe complement signal on the AGP bus.

8. (Amended) An apparatus [system], comprising:
a graphics bus;
a graphics device coupled to the graphics bus, the graphics device including
a bus interface unit including a plurality of bus signal buffers to couple the graphics device to the graphics bus, and
a load balancing bus signal buffer to further couple the graphics device to the graphics bus, the load balancing bus signal buffer to provide load balancing on the graphics bus when a second graphics device is installed; and
a second graphics device connector to receive a second graphics device, the second graphics device connector to couple the second graphics device to the graphics bus.

9. (Amended) The apparatus [system] of claim 8, wherein the graphics bus is an accelerated graphics port (AGP) bus.

10. (Amended) The apparatus [system] of claim 9, wherein the graphics device is an AGP 2X device.

11. (Amended) The apparatus [system] of claim 10, the upgrade graphics device connector to receive an AGP 4X device.

12. (Amended) The apparatus [system] of claim 11, the load balancing bus signal buffer to provide load balancing for a first address/data bus strobe compliment signal on the AGP bus.

13. (Amended) The apparatus [system] of claim 11, the load balancing bus signal buffer to provide load balancing for a second address/data bus strobe compliment signal on the AGP bus.

14. (Amended) The apparatus [system] of claim 11, the load balancing bus signal buffer to provide load balancing for a sideband strobe compliment signal on the AGP bus.

15. (Amended) A method, comprising:
coupling a graphics device to a graphics bus, the graphics device including [a bus interface unit, the bus interface unit including] a plurality of bus signal buffers to couple the graphics device to the graphics bus; and
providing a load balancing bus signal buffer to further couple the graphics device to the graphics bus, the load balancing bus signal buffer to provide load balancing on the graphics bus when an upgrade graphics device is installed.

16. (Amended) The method of claim 15, wherein [the step of] providing a load balancing bus signal buffer includes the step of providing a load balancing

bus signal buffer for an address/data bus strobe compliment signal on an accelerated graphics port (AGP) bus.

17. (Amended) The method of claim 15, wherein [the step of] providing a load balancing bus signal buffer includes the step of providing a load balancing bus signal buffer for a sideband strobe compliment signal on an AGP bus.